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Development and Optimization of Integrative MEMS-Based Gray-Scale Technology In Silicon For Power MEMS Applications

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DEVELOPMENT AND OPTIMIZATION OF INTEGRATIVE MEMS-BASED GRAY-SCALE TECHNOLOGY IN SILICON FOR POWER MEMS APPLICATIONS

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ABSTRACT

As the field of micro-electro-mechanical systems (MEMS) has diversified, a growing number of applications are limited by the current planar technology available for fabrication. Gray-scale technology offers a method of fabricating 3-D structures in MEMS utilizing a single lithography step. Before gray-scale technology can be accepted as a universal/standard fabrication technique, methods for controlling the silicon profiles and integrating the necessary process steps must be developed. Here, an optical mask design method is outlined by which an arbitrary profile may be defined in a photoresist film, and a study is presented regarding the control of etch selectivity during deep reactive ion etching (DRIE). These results are then used to develop large controlled gradient silicon structures for the MIT micro-engine device that may be integrated into an existing process flow.

INTRODUCTION

Micro-electro mechanical systems (MEMS) have the potential to provide high-performance, lightweight power generation systems [1,2]. However, to this point MEMS designers have been severely restricted when attempting to expand their systems in the vertical domain, often utilizing only planar or 2-dimensional technologies. If precise 3-dimensional (3D) structures could be developed and integrated into standard process flows, proposed systems such as the MIT micro-engine device could utilize this fabrication technique to routinely mimic their macro counterparts to achieve high efficiency. Specifically, creating a sloped, rather than planar, micro-compressor could improve engine efficiency.

Techniques to fabricate various 3D structures have been developed in the past, however they are limited in the range of possible profiles, are not repeatable, or require multiple fabrication steps [3-5]. However, recently gray-scale technology, a technique commonly used in diffractive optics [6-9], has been extended to provide arbitrary gradient height profiles in silicon MEMS structures [10-14]. One of the primary advantages of using gray-scale technology to create 3D structures is that only one lithography and etching step are necessary. Therefore, applications that require large sloped profiles to achieve high performance, such as a MEMS micro-compressor, could benefit from gray-scale technology.

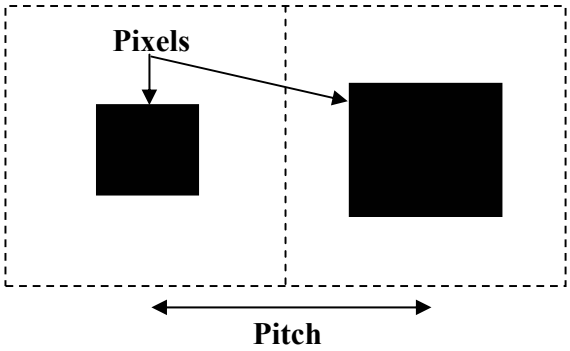

Fig. 1: Sub-resolution pixels are spaced with a sub-resolution pitch. The transmission through the optical mask (Tr) is proportional to the relative areas of the pixel and pitch.

Gray-scale technology consists of two key steps: first, the formation of a 3D photoresist pattern using a specially designed gray-scale optical mask, and second, the subsequent transfer of this structure into silicon using deep reactive ion etching (DRIE). Although, only a single lithography step is required to create a 3D pattern, the design and processing steps must be tightly controlled.

The optical mask is designed using a large number of sub-resolution opaque pixels spaced with a fixed sub-resolution pitch (see Fig. 1). Since both, pixel and pitch, sizes are below the resolution of the projection lithography system being used; the actual shape of the pixel is trivial. It is only the area the pixel occupies within the pitch that is important, determining the relative amount of light that is blocked, creating an intermediate intensity (between 0 and 100%) or gray level. Thus, during a single exposure, a photoresist film is exposed to different depths depending on the amount of light received at each location. During development the exposed portions of the photoresist will be washed away, creating a variable height photoresist

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structure corresponding to the intensity pattern generated by the optical mask. The development step must be tightly controlled because over-development will cause extra photoresist to be washed away and the loss of gray levels.

Once the desired 3D pattern is created in photoresist, selective etching in a DRIE system transfers this pattern into the photoresist. The etch selectivity (relative etch rate of silicon to photoresist) during the DRIE process determines the scaling factor of the vertical dimensions of the photoresist structure. It is therefore extremely important to control the etch selectivity during the DRIE process in order to create 3D structures with precisely defined vertical dimensions.

One of the great challenges to gray-scale technology is that of uniformity because the photoresist processing must be tightly controlled to create identical structures across the wafer. This non-uniformity present in the photoresist was shown to be amplified during DRIE pattern transfer by approximately the etch selectivity [15]. In this paper we will describe the steps taken to define a photoresist profile to resemble virtually any desired function, as well as a characterization of DRIE etch characteristics for coarse tuning of etch selectivity to define the vertical dimensions. The integration of these processes into an existing process flow for the MIT micro engine device is then proposed and developed.

GRAY-SCALE OPTICAL MASK DESIGN

The inherent nature of gray-scale technology requires that gray-scale masks for structures of appreciable size be made with $>10^6$ pixels or more. Depending on the geometry of a particular application, mask design may be simplified by repeating fundamental elements in arrays. However, for gray-scale technology to become an integrative technology, the design and fabrication restrictions must be few. Therefore, an automated method must be developed to individually define the large number of pixels required to create a structure.

The first step to creating such a design methodology is to define and optimize the lithography process using a calibration mask with simple structures [12]. This optimum process is then fixed and considered a constant. Profilometer measurements are then taken of various structures made from known pixel sizes within the given pitch. The transmission through the optical mask (*Tr*) is then calculated by:

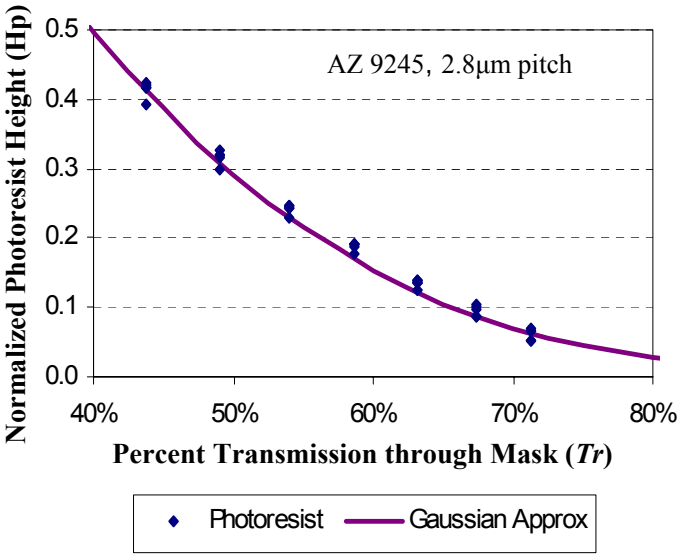

Fig. 2: A Gaussian curve is used to approximately relate the measured normalized height in photoresist (Hp) to the percent transmission through the optical mask (Tr). ©IEEE 2004

$$Tr = 1 - \frac{A_{pixel}}{A_{pitch}} \qquad (1)$$

The photoresist height can then be plotted versus the transmission for a few various size pixels across a desired range, as shown in Figure 2. Since the contrast curve of most photoresist films resembles an exponential or Gaussian function, the measured data points can be approximated with a Gaussian curve using two fit parameters A_0 and γ [13]:

$$H_P = A_0 * \exp\left(-(Tr)^2 * \gamma\right) \qquad (2)$$

This Gaussian approximation can be easily inverted so the desired height at a particular location can be used to calculate the necessary transmission through the optical mask:

$$Tr = \sqrt{\frac{-\ln\left(\frac{H_P}{A_0}\right)}{\gamma}} \qquad (3)$$

To design a device, the user must first create the set of pixels they wish to use (within any restrictions set by their optical mask vendor) creating a discrete set of available transmissions. A function defining the desired profile can then be input into equation (3) above to calculate the ideal transmission at every point on a design, which is then rounded to the nearest available transmission to select the appropriate pixel.

This method has been used to create the desired linear profile on a micro-compressor. Previously, the available levels were evenly distributed over the design, resulting in a profile resembling an exponential (shown later in Fig.

Parameter	Silicon Loading (%)	Selectivity	Si Etch Rate (μm/cycle)	PR Etch Rate (μm/cycle)	Sidewall Angle (Inside/Outside)
Base Etch	42	75	0.71	0.010	-0.1˚/-2.0˚
High Silicon Loading	57	42	0.73	0.016	-0.1˚/-2.0˚
Low Silicon Loading	27	92	0.90	0.010	-0.3˚/-2.1˚
Oxygen Step	42	30	0.46	0.014	-0.6˚/-2.0˚
High Electrode Power	42	55	0.71	0.013	-0.5˚/-2.1˚
Low Electrode Power	42	103	0.54	0.005	2.3˚/0.4˚
Increased Temperature	42	48	0.75	0.015	-1.3˚/-2.9˚

Table 1. The effects of each parameter investigated on selectivity, silicon etch rate, and profile.

4). By inputting a linear profile into the Gaussian approximation mask design method, each location was given the optimum pixel, creating a linear slope (shown later in Fig. 5).

ETCH SELECTIVITY CONTROL

As mentioned before, etch selectivity must be investigated in order to precisely fabricate deep profiles in silicon. Versatility in etch selectivity can allow wide range of photoresist thicknesses to be used (which may ease lithography processing), as well as enable a multitude of final silicon gray-scale structure height.

The etch selectivity not only controls the final vertical dimensions, but also the surface morphology of the gray levels themselves. When transferring the gray levels into the silicon, the photoresist defining the height profile is fully transferred including the surface morphology. Any surface roughness or non-uniformity present on the photoresist surface is then magnified by the etch selectivity. For example, the average photoresist surface roughness has been measured to be below 30nm. When etched using an etch selectivity of 24, the silicon surface roughness became ~1600nm, whereas an etch selectivity of 14 resulted in a silicon surface roughness of ~360nm. It is then apparent that a small etch selectivity is beneficial to minimize any magnification of the photoresist surface roughness and non-uniformity.

Effects of the main DRIE etch parameters were investigated to obtain a wide range of etch selectivities, where the etch selectivity is the relative etch rate of silicon to photoresist. The primary etching mechanism of silicon in DRIE is chemical etching, while the primary etching mechanism of photoresist is ion sputtering. We have investigated changes in electrode power, temperature, amount of exposed silicon (loading), and an additional oxygen step, in an attempt to vary the relative etch rates of silicon and photoresist to obtain different selectivities[16]. The etch characteristics of our investigation are given in Table 1.

The significance of Table 1 is that it allows a starting point to be established for etching photoresist gray levels with various heights to different depths in silicon. Although, these are useful for coarse control of etch selectivity, further investigation will be necessary to achieve precise control over the etch selectivity, and more importantly, to maintain a process with consistent etch selectivity. It must be noted that during photoresist pattern transfer, the silicon loading will gradually increase as the photoresist is removed, causing the etch selectivity to decrease during the course of an etch.

MICRO-COMPRESSOR AND PROCESS INTEGRATION

The focus of gray-scale technology for the micro-gas turbine engine at MIT has been reported by the authors in [15]. As mentioned in the previous publication, the development of a micro-gas turbine engine requires an efficient compressor design, but current designs have been limited to planar structures using conventional microfabrication techniques. A complex three-dimensional compressor design that improves engine cycle performance incorporates a variable height flow passage. This improved design can be accomplished using gray-scale lithography and DRIE.

A first demonstration of a complex 3D compressor is shown in Fig. 3. To obtain a desired height of 200μm in silicon for the outer-sloped region, the photoresist thickness at the outer-sloped region must be measured so the necessary etch selectivity can be found. For one sample, the photoresist was measured to be an average of 3μm at that outer region so that a selectivity of 67 was needed. When using the base etch I from Table 1 a height of 210μm was achieved. The height of the blades in Fig. 3 is a constant 350μm above the base of the etched silicon.

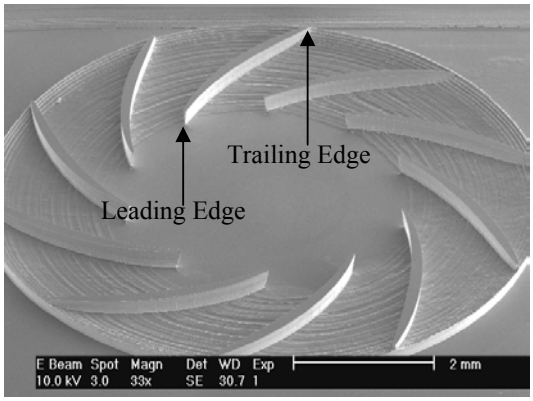

Fig. 3: Variable height micro-compressor in silicon showing the leading edge etched 350μm and the trailing edge etched 140μm.

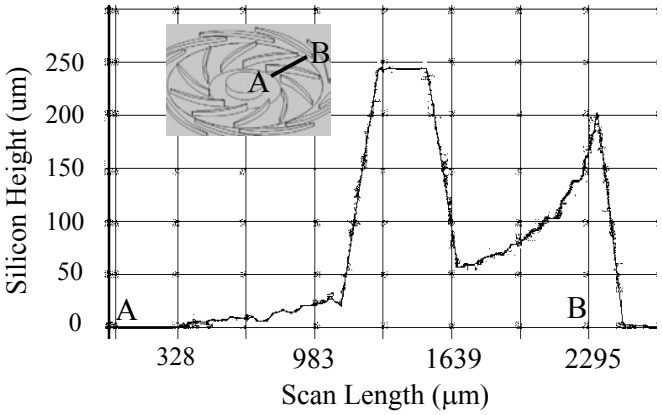

Figure 4: Contact profilometer scan showing the profile of the compressor with the height of the blade being 245μm and the height of the slope peaking at 200μm. The scan goes from A to B in the diagram.

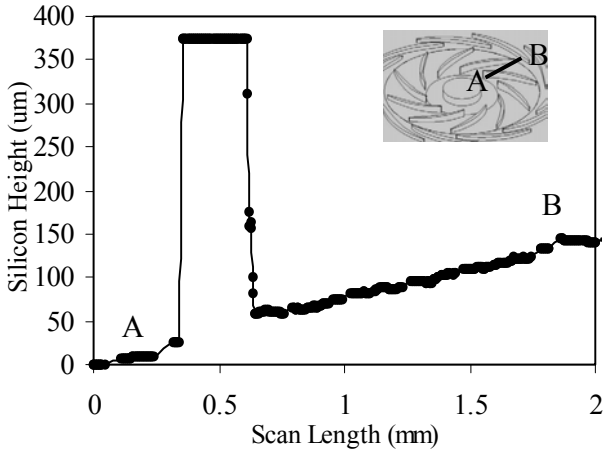

Fig. 5: Optical profilometer scan showing a modified profile design fabricated in silicon for a linear profile. The outer sloped height is ~150μm obtained from an etch selectivity of 83 from a photoresist height of ~1.8μm. The scan goes from A to B.

Fig. 4 shows the profile of the fabricated micro-compressor from a contact profilometer scan. It is apparent that in this demonstration, the sloped is non-linear, of which the desired is linear. By using the Guassian approximation method, a 2nd design was fabricated with the appropriate pixels for a linear slope. The profile of the modified design is shown in Fig. 5, obtained through an optical profilometer scan.

The entire micro-compressor, including the outer and inner blades can be fabricated in one gray-scale lithography and etch step. This has been demonstrated, and this design is the source of the profile shown in Fig. 5. To fabricate such a design, a large single gray level (12mm x 12mm) was used to define the flat flow passage beneath the outer static blades. Due to the transfer of photoresist non-uniformity and surface roughness and their amplification during DRIE, the single gray level exhibits surface roughness greater than 1μm, and height differences greater than 3μm.

An integration process is thus proposed to eliminate the effects of photoresist surface roughness and non-uniformity on the large flow passage area beneath the outer static blades. Fig. 6 shows the new process using a silicon dioxide nested mask so that etching is performed in a two-step process, eliminating the need for a large single gray level.

Fig. 6(a) shows a cross-section of the MIT wafer as it currently appears in their fabrication flow. To create a planar micro-compressor, a single DRIE step is used to etch the regions between the thermal oxide and silicon nitride features. With the addition of the steps shown in Fig. 6(b)-(e), a variable height compressor may be fabricated.

First, in Fig. 6(b), plasma enhanced chemical vapor deposition (PECVD) is used to deposit a second silicon dioxide layer, which is patterned using traditional lithography. A thick photoresist film is then spun on top of the entire wafer, and patterned using gray-scale lithography only over the micro-compressor. DRIE is then used to transfer this pattern into the silicon, only creating a slope on the micro-compressor. The remaining photoresist is then stripped away, shown in Fig. 6(c), exposing the patterned PECVD oxide layer. This oxide layer can then be used as a mask in DRIE to transfer the sloped profile further into the silicon while etching the flat, large flow channel beneath the outer static blades, resulting in Fig. 6(e). The PECVD oxide layer is removed, followed by the silicon nitride layer, Fig. 6(f).

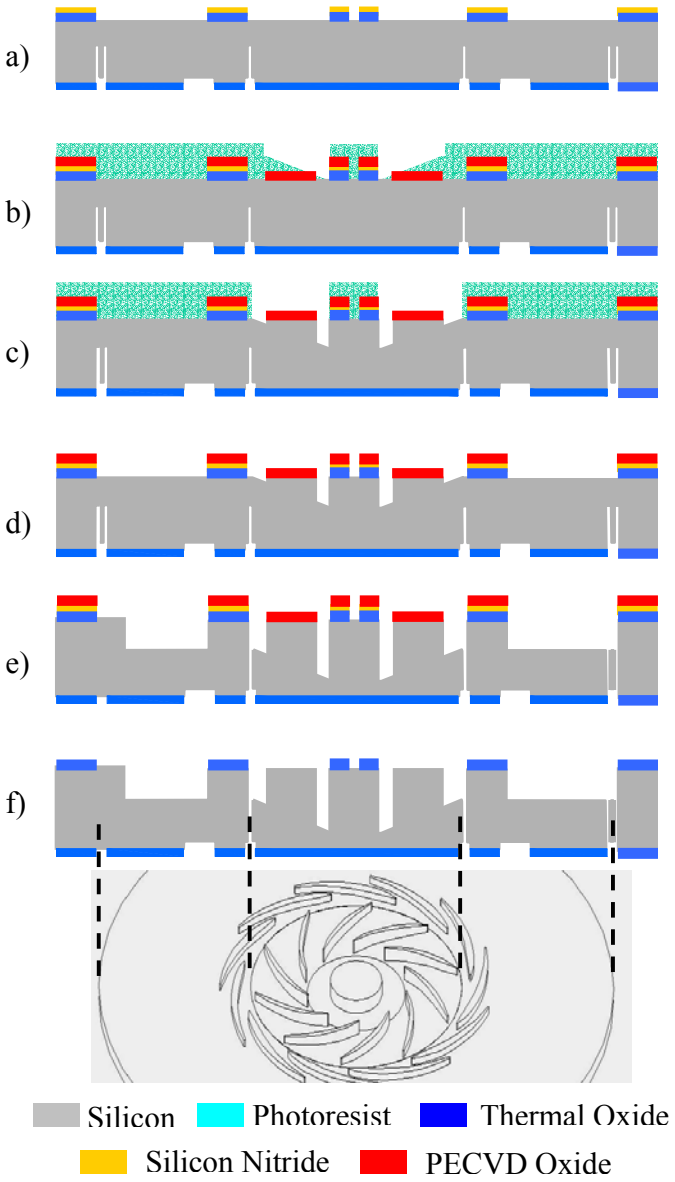

Fig. 6: Process steps using a silicon dioxide nested mask to integrate the gray-scale patterned micro-compressor into the current process steps of the MIT micro-gas turbine engine.

The final structure shown in Fig. 6(f) exhibits a sloped micro-compressor that leads to a large, flat flow channel beneath the outer static blades. If gray-scale technology had not been used, the profile in Fig. 6(f) would have a flat micro-compressor etched to the identical depth as the outer flow channels.

The fabrication process shown in Fig. 6 is currently under development. The major challenge for developing such a process will again be photoresist non-uniformity. Since the thick photoresist film must be spun over 3 patterned layers on top of the silicon, a certain degree of non-uniformity should be expected. It is possible that thicker photoresist layers, or multiple photoresist spins may alleviate the problem, and are currently being investigated.

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CONCLUSIONS

A gray-scale technology capable of producing repeatable 3D structures in silicon will have many benefits in the area of microfabrication, enabling microstructures that closely resemble their macroscopic counterparts. Three primary challenges have thus been investigated herein towards this end: a method of designing an arbitrary photoresist profile was developed, techniques for tuning of the etch selectivity during DRIE were presented, and an example was given of how a gray-scale process could be integrated into an existing process flow. Thus, large 3-D silicon structures in power MEMS applications, such as the MIT micro turbine engine device, could be significantly improved with the newfound capability of creating sloped silicon profiles using gray-scale technology.

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